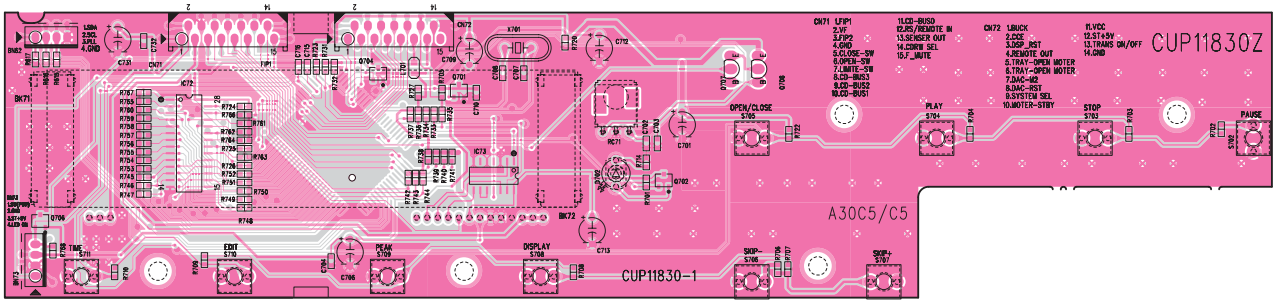
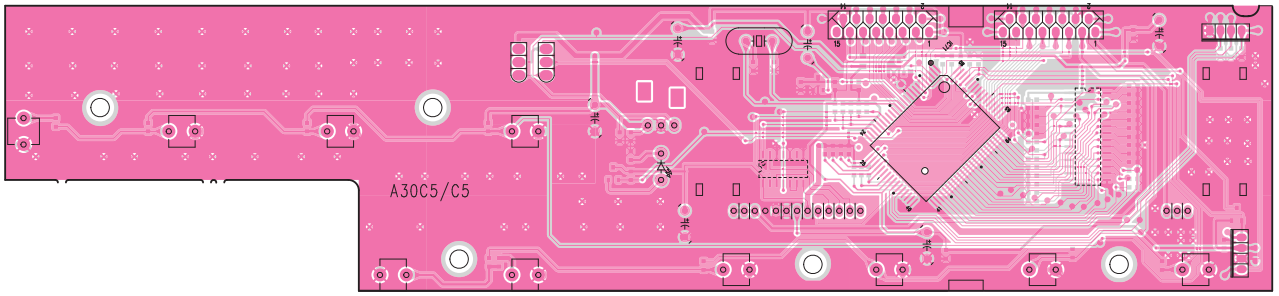
FRONT A

Q706 IC72 Q704 Q701 IC73 Q702 Q707 Q708



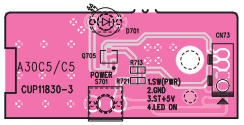
FRONT B

IC71

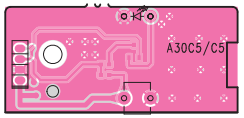


POWER SW A

Q705



POWER SW B



鉛フリー半田

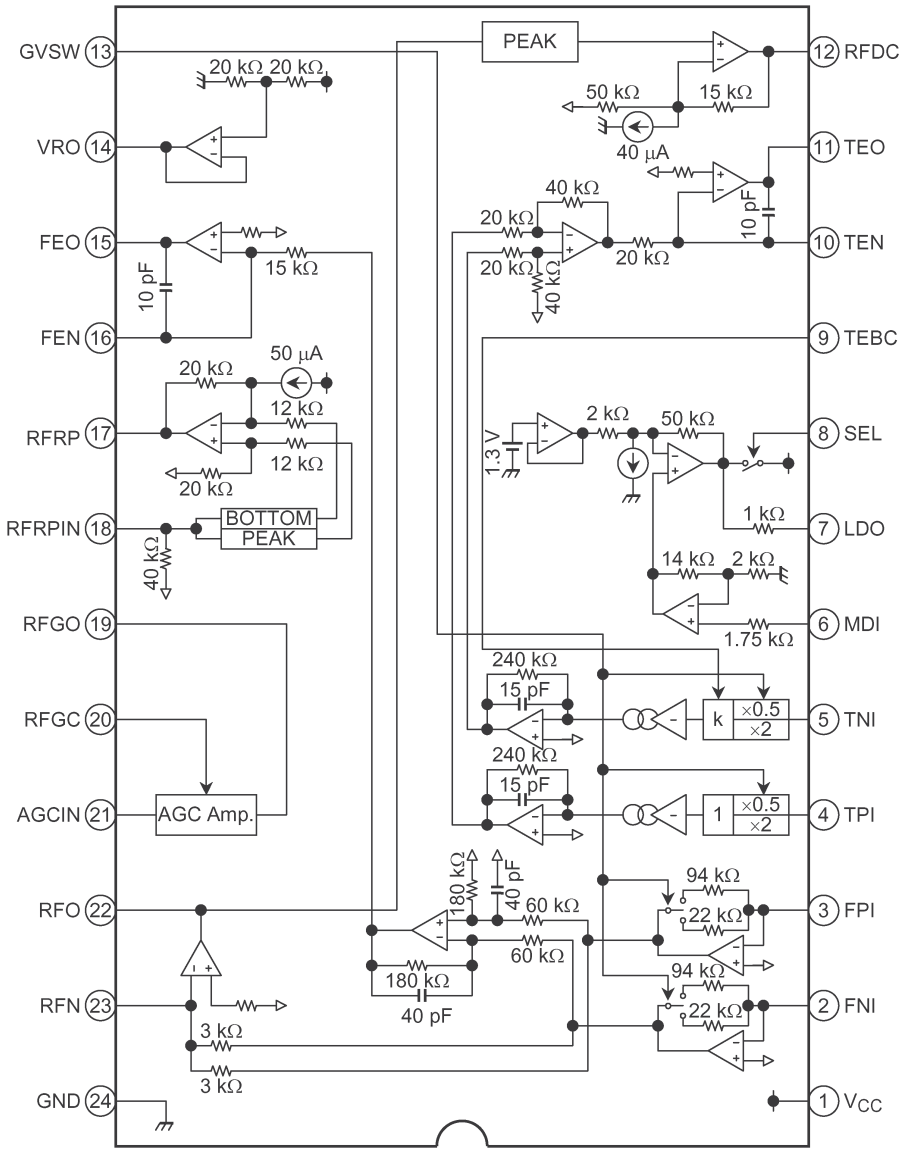
半田付けには、鉛フリー半田 (Sn-Ag-Cu) を使用してください。

Lead-free Solder

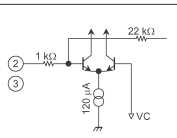
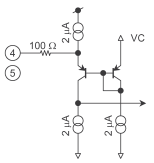
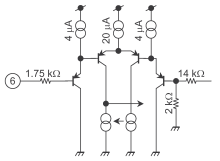
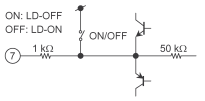
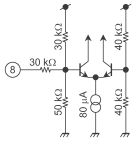
When soldering, use the Lead-free Solder (Sn-Ag-Cu).

9. MICROPROCESSOR AND IC DATA

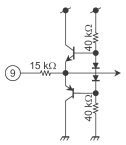
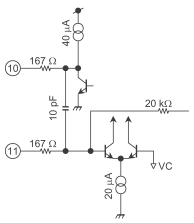
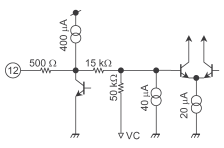
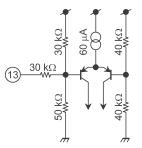
IC11 : TA2157FN



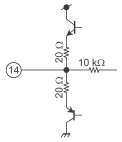
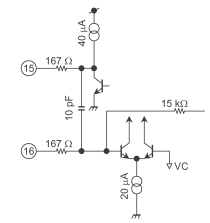
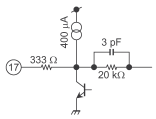
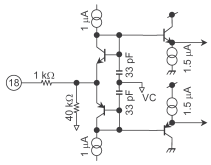
IC11 : TA2157FN

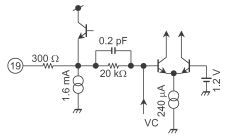
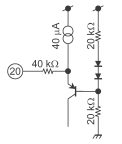
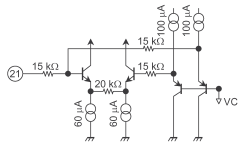
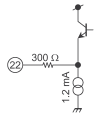
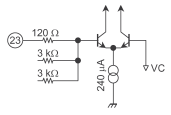
Pin No.	Symbol	I/O	Function Description	Internal Circuit
1	V_{CC}	—	3.3 V power supply pin	—
2	FNI	I	Main-beam amp input pin	
3	FPI	I	Main-beam amp input pin	
4	TPI	I	Sub-beam amp input pin	
5	TNI	I	Sub-beam amp input pin	
6	MDI	I	Monitor photo diode amp input pin	
7	LDO	O	Laser diode amp output pin	
8	SEL	I	APC circuit ON/OFF control signal, laser diode (LDO) control signal input or bottom/peak detection frequency change pin.	

SEL	APC Circuit	LDO
GND	OFF	Connected to V_{CC} through 1 kΩ resistor
HiZ	ON	Control signal output
V_{CC}	ON	Control signal output

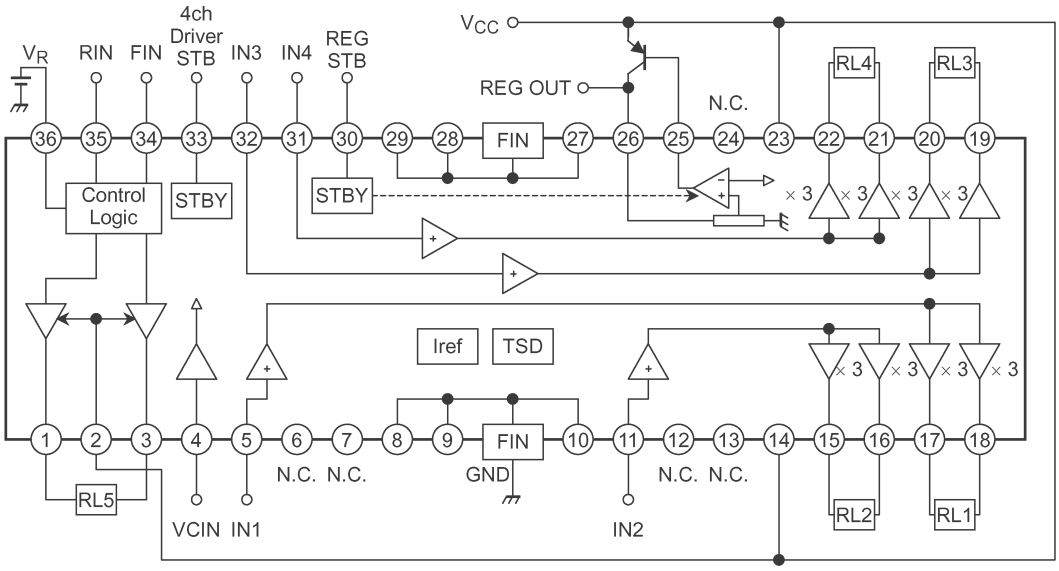
Pin No.	Symbol	I/O	Function Description	Internal Circuit
9	TEBC	I	Tracking error balance adjustment signal input pin Adjusts TE signal balance by eliminating carrier component from PWM signal (3-state output, PWM carrier = 88.2 kHz) output from TC94A14F/FA/FB TEBC pin using RC-LPF and inputting DC. TEBC input voltage: GND~V_{CC}	
10	TEN	I	Tracking error signal generation amp negative-phase input pin	
11	TEO	O	Tracking error signal generation amp output pin. Combining TEO signal and RFRP signal with TC94A14F/FA/FB configures tracking search system.	
12	RFDC	O	RF signal peak detection output pin	
13	GVSW	I	AGC/FE/TE amp gain change pin	

GVSW	Mode
GND	CD-RW
HiZ	Normal
V_{CC}	

Pin No.	Symbol	I/O	Function Description	Internal Circuit
14	VRO	O	Reference voltage (VRO) output pin • VRO = 1/2 V_{CC} when V_{CC} = 3.3 V	
15	FEO	O	Focus error signal generation amp output pin	
16	FEN	I	Focus error signal generation amp negative-phase input pin	
17	RFRP	O	Signal amp output pin for track count Combining RFRP signal and TEO signal with TC94A14F/FA/FB configures tracking search system.	
18	RFRPIN	I	Signal generation amp input pin for track count	

Pin No.	Symbol	I/O	Function Description	Internal Circuit
19	RFGO	O	RF signal amplitude adjustment amp output pin	
20	RFGC	I	RF amplitude adjustment control signal input pin Adjusts RF signal amplitude by eliminating carrier component from PWM signal (3-state output, PWM carrier = 88.2 kHz) output from TC94A14F/FA/FB RFGC pin using RC-LPF and inputting DC. • RFGC input voltage : GND~V_{CC}	
21	AGCIN	I	RF signal amplitude adjustment amp input pin	
22	RFO	O	RF signal generation amp output pin	
23	RFN	I	RF signal generation amp input pin	
24	GND	—	GND pin	—

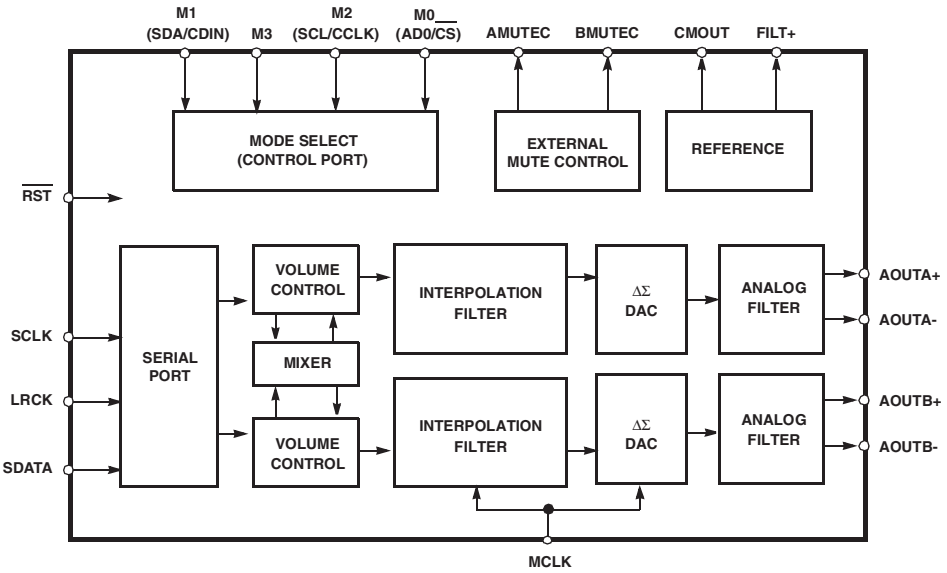
IC13 : TA2125AF

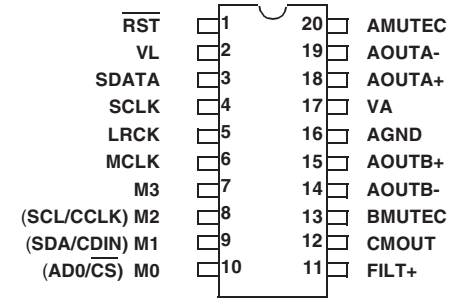


IC13 : TA2125AF

No.	Symbol	Function	
1	OUT5A	Output terminal	H-bridge
2	V_M	Supply voltage terminal for Logic	H-bridge
3	OUT5B	Output terminal	H-bridge
4	V_{CIN}	Input reference voltage	4ch BTL
5	IN1	Input for ch1	4ch BTL
6	N.C.	Open	—
7	N.C.	Open	—
8	N.C.	8, 9, 10, 27, 28, 29 are connected to PW GND (FIN)	—
9	N.C.	8, 9, 10, 27, 28, 29 are connected to PW GND (FIN)	—
10	N.C.	8, 9, 10, 27, 28, 29 are connected to PW GND (FIN)	—
11	IN2	Input for ch2	4ch BTL
12	N.C.	Open	—
13	N.C.	Open	—
14	V_{CC1}	Supply voltage terminal for ch1/ch2	4ch BTL
15	OUT2M	Inverted output for ch2	4ch BTL
16	OUT2P	Non-inverted output for ch2	4ch BTL
17	OUT1M	Inverted output for ch1	4ch BTL
18	OUT1P	Non-inverted output for ch1	4ch BTL
19	OUT3P	Non-inverted output for ch3	4ch BTL
20	OUT3M	Inverted output for ch3	4ch BTL
21	OUT4P	Non-inverted output for ch4	4ch BTL
22	OUT4M	Inverted output for ch4	4ch BTL
23	V_{CC2}	Supply voltage terminal for ch3/ch4	4ch BTL
24	N.C.	Open	—
25	REG	Connection with BASE of PNP Tr	Regulator
26	REG OUT	Output for regulator (5 V)	Regulator
27	N.C.	8, 9, 10, 27, 28, 29 are connected to PW GND (FIN)	—
28	N.C.	8, 9, 10, 27, 28, 29 are connected to PW GND (FIN)	—
29	N.C.	8, 9, 10, 27, 28, 29 are connected to PW GND (FIN)	—
30	REG STBY	Standby control for regulator	Regulator
31	IN4	Input for ch4	4ch BTL
32	IN3	Input for ch3	4ch BTL
33	STBY	Standby control for 4ch BTL	4ch BTL
34	FIN	Logic control input	H-bridge
35	RIN	Logic control input	H-bridge
36	VR	Supply voltage terminal for motor driver	H-bridge

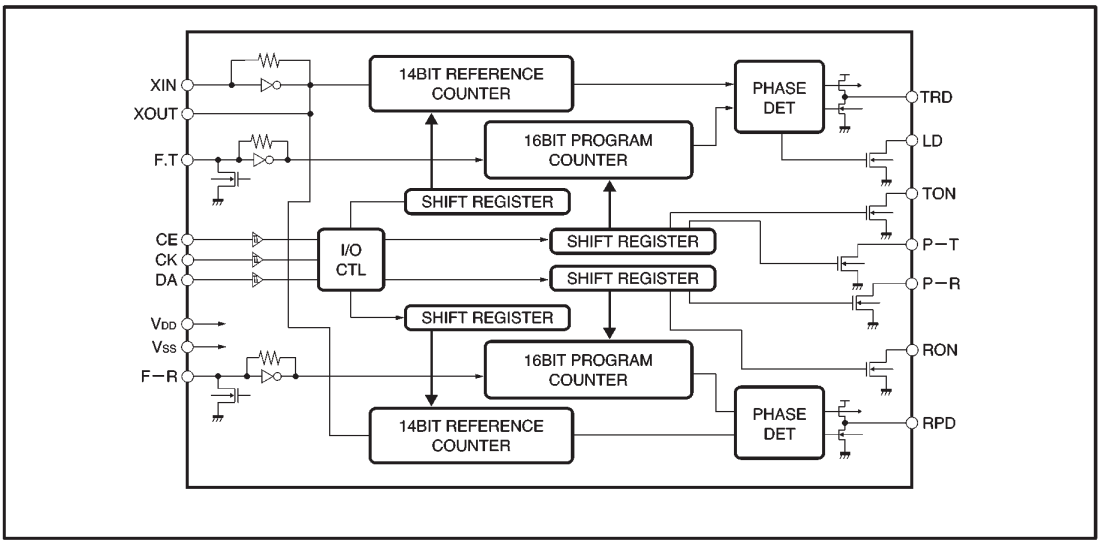
IC14 : CS4392KS





RST	1	**Reset** (*Input*) - Powers down device and resets all internal registers to their default settings.
VL	2	**Logic Power** (*Input*) **-** Positive power for the digital input/output.
SDATA	3	**Serial Audio Data** (*Input*) - Input for two's complement serial audio data.
SCLK	4	**Serial Clock** (*Input/Output*) - Serial clock for the serial audio interface.
LRCK	5	**Left Right Clock** (*Input/Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
MCLK	6	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
FILT+	11	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.
CMOUT	12	**Common Mode Voltage** (*Output*) - Filter connection for internal quiescent voltage.
AMUTEC **BMUTEC**	20 13	**Mute Control** (*Output*) - The Mute Control pin goes high during power-up initialization, reset, muting, power-down or if the master clock to left/right clock frequency ratio is incorrect.
AOUTB- **AOUTB+** **AOUTA+** **AOUTA**	14 15 18 19	**Differential Analog Output** (*Outputs*) - The full scale differential analog output level is specified in the Analog Characteristics specification table.
AGND	16	**Ground** (*Input*)
VA	17	**Analog Power** (*Input*) **-** Positive power for the analog section.
Control Port Mode Definitions		
M3	7	**Mode Selection** (*Input*) - This pins should be tied to GND level during control port mode.
SCL/CCLK	8	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port.
SDA/CDIN	9	**Serial Control Data** (*Input/Output*) - SDA is a data I/O line in I^2C mode. CDIN is the input data line for the control port interface in SPI mode.
AD0/$\overline{CS}$	10	**Address Bit 0 (I^2C) / Control Port Chip Select (SPI)** (*Input/Output*) - AD0 is a chip address pin in I^2C mode; $\overline{CS}$ is the chip select signal for SPI format.
Stand-Alone Mode Definitions		
M3 **M2** **M1** **M0**	7 8 9 10	**Mode Selection** (*Input*) - Determines the operational mode of the device.

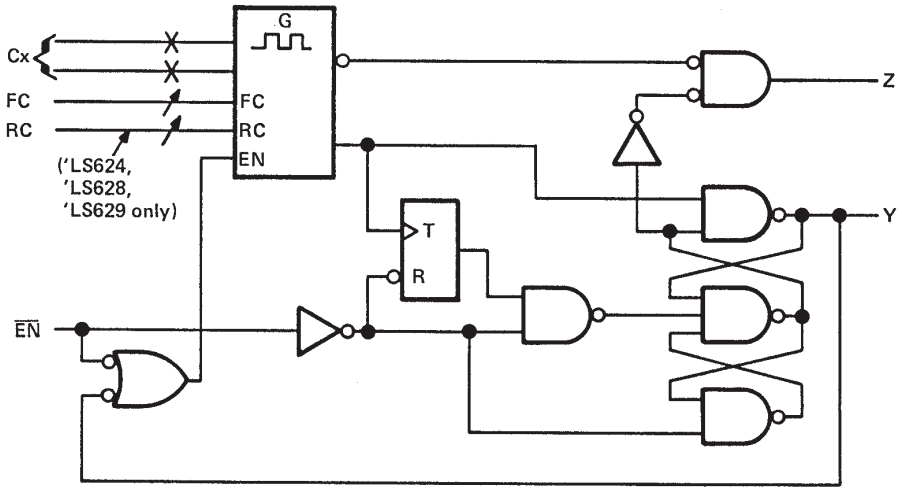
IC61 : BU2630



Pin No.	Pin name	Name	Function	I/O cuircuit
16	XOUT	Crystal resonator	For reference frequency	TYPE A
1	XIN			
2	V_{SS}			
3	RPD	Phase comparator output	This is LO if the locally divided value is higher than the reference frequency, HI if it is lower, and Z if it matches.	TYPE E
4	P−R	Output port	This is controlled by the input data.	TYPE D
5	RON			
6	F−R	VCO input	Local input for reception	TYPE F
7	CE	Chip enable clock signal serial data	When CE is HIGH, the DA synchronized to the rise of CK is read into the internal shift register, and is latched at the timing of the CE fall.	TYPE B
8	CK			
9	DA			
10	LD	Unlock output	This goes ON when the PLL is unlocked on the transmission side	TYPE D
11	F−T	VCO input	Local input for transmission	TYPE F
12	TON	Output port	This is controlled by the input data	TYPE D
13	P−T			
14	TPD	Phase comparator output	This is LO if the locally divided value is higher than the reference frequency, HI if it is lower, and Z if it matches.	TYPE E
15	V_{DD}	Power supply	2.5~5.5V	

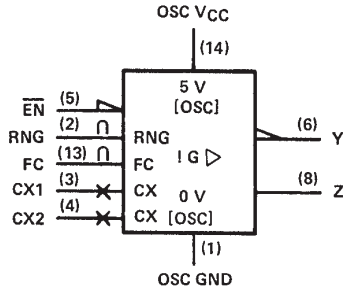
IC62 : TC74LS628

logic diagram (positive logic)

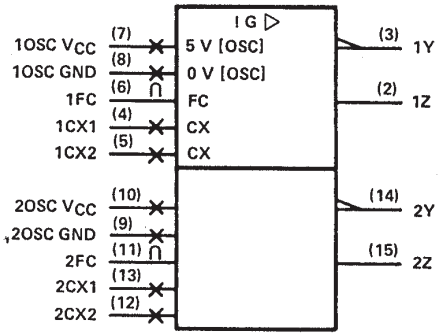


logic symbols†

'LS624



'LS625



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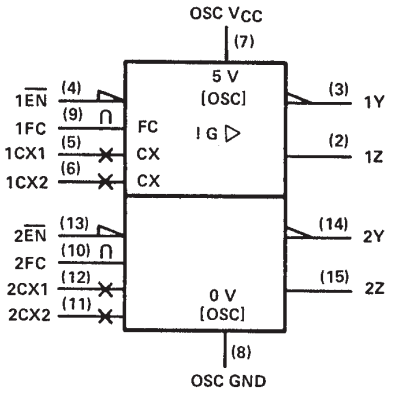
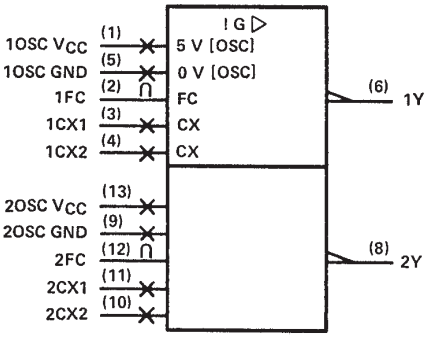


'LS627



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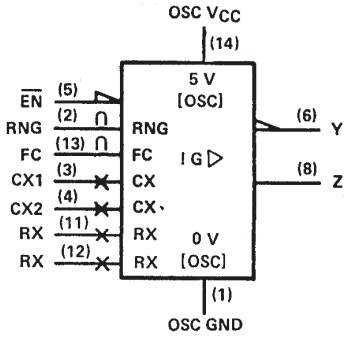
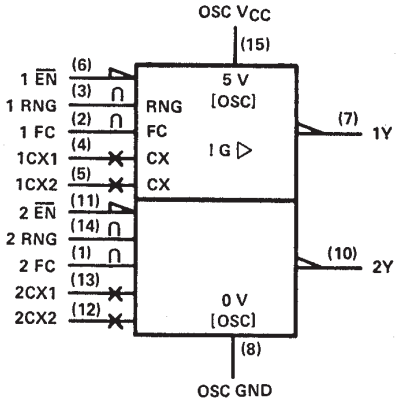


'LS629



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.